

21  
**PATENT**

Attorney Docket 3846.2US (98-0796.2)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL740531244US  
Date of Deposit with USPS: April 9, 2001  
Person making Deposit: Daniel Thatcher

APPLICATION FOR LETTERS PATENT

for

**WAFER-LEVEL PACKAGE AND METHODS OF FABRICATING**

Inventors:  
Salman Akram  
Alan G. Wood

Attorneys:  
Brick G. Power  
Registration No. 38,581  
James R. Duzan  
Registration No. 28,393  
TRASKBRITT  
P.O. Box 2550  
Salt Lake City, Utah 84110  
(801) 532-1922

# WAFER-LEVEL PACKAGE AND METHODS OF FABRICATING

Sub A1 >

## CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** This application is a continuation of application Serial No. 09/340,513, filed June 28, 1999 pending.

## BACKGROUND OF THE INVENTION

**[0002]** Field of the Invention: The present invention relates to carrier substrates for use in chip-scale packages and to chip-scale packages including such carrier substrates. Particularly, the present invention relates to carrier substrates fabricated from polymeric materials. Methods of fabricating chip-scale packages are also within the scope of the present invention.

**[0003]** Background of Related Art: In conventional semiconductor device fabrication processes, a number of distinct semiconductor devices, such as memory chips or microprocessors, are fabricated on a semiconductor substrate, such as a silicon wafer. After the desired structures, circuitry, and other features of each of the semiconductor devices have been fabricated upon the semiconductor substrate, the substrate is typically singulated to separate the individual semiconductor devices from one another.

**[0004]** Various post-fabrication processes, such as testing the circuits of each of the semiconductor devices and burn-in processes, may be employed either prior to or following singulation of the semiconductor substrate. These post-fabrication processes may be employed to impart the semiconductor devices with their intended functionality and to determine whether or not each of the individual semiconductor devices meets quality control specifications.

**[0005]** The individual semiconductor devices may then be packaged. Along with the trend in the semiconductor industry to decrease semiconductor device size and increase the density of structures of semiconductor devices, package sizes are also ever-decreasing. One type of semiconductor device package, the so-called "chip-scale package" or "chip-sized package" ("CSP"), consumes about the same amount of real estate upon a substrate as the bare semiconductor device itself. Such chip-scale packages typically include a carrier substrate having roughly the same surface area as the semiconductor device.

**[0006]** Some chip-scale packages include a semiconductor device and a polymeric carrier substrate. Exemplary chip-scale packages with polymeric carrier substrates are disclosed in United States Patent 5,677,576 (hereinafter “the ‘576 Patent”), which issued to Masatoshi Akagawa on October 14, 1997, United States Patent 5,683,942 (hereinafter “the ‘942 Patent”), which issued to Keiichiro Kata et al. on November 4, 1997, and United States Patent 5,844,304 (hereinafter “the ‘304 Patent”), which issued to Keiichiro Kata et al. on December 1, 1998.

**[0007]** The ‘576 Patent discloses a chip-scale package that includes a semiconductor device, a layer of insulative material, through which bond pads of the semiconductor device are exposed, disposed on an active surface of the semiconductor device, and a conductive elastomer disposed adjacent the layer of insulative material and the bond pads of the semiconductor device. Conductive elements are positioned adjacent the conductive elastomer so as to facilitate the disposition of a conductive bump that is laterally offset from the bond pad location. A photoresist, including apertures through which portions of the conductive elements are exposed, is then disposed over the conductive elements and the conductive elastomer. Conductive bumps are disposed within the apertures and in communication with the conductive elements. The carrier substrate and method of the ‘576 Patent are somewhat undesirable because the disposal of an additional layer of insulative material on the active surface of the semiconductor device may increase fabrication time and costs, as well as the likelihood of device failure. Moreover, as each of the bond pads is associated with a laterally extending conductive element, each of the conductive bumps is, somewhat undesirably, laterally offset from the location of its corresponding bond pad.

**[0008]** The ‘942 Patent describes a carrier substrate including a polymer layer including conductive traces with raised contact pads disposed on a first side thereof and corresponding conductive bumps disposed on the other side thereof. The conductive traces and their corresponding conductive bumps communicate by means of electrically conductive vias through the carrier substrate. A layer of insulative material is disposed upon the active surface of the semiconductor device with which the carrier substrate is to be assembled, laterally adjacent the bond pads. The carrier substrate, which is pre-fabricated, is disposed adjacent the active surface of a semiconductor device by aligning the contact pads of the carrier substrate with the bond pads

of the semiconductor device, disposing a quantity of adhesive material between the active surface and the carrier substrate, and applying pressure to the carrier substrate to abut the contact pads against their corresponding bond pads. Pressure is applied locally to the contact pads and, thus, to the bond pads through apertures defined through the carrier substrate. The carrier substrate of the '942 Patent is somewhat undesirable in several respects. The disposal of a layer of insulative material laterally adjacent the bond pads of the semiconductor device increases fabrication time and costs, as well as the likelihood of device failure. The semiconductor device may be damaged while localized pressure is applied to the bond pads thereof, again undesirably increasing the likelihood of device failure and, therefore, fabrication costs. Moreover, since the carrier substrate of the '942 Patent is pre-fabricated, it is possible that the raised contact pads of the carrier substrate may not properly align with their corresponding bond pads of the semiconductor device.

**[0009]** The polymeric carrier substrate of the '304 Patent is fabricated directly upon an active surface of a semiconductor device. That carrier substrate, however, does not include electrically conductive vias that extend substantially longitudinally therethrough. Rather, a layer of insulative material is disposed on an active surface of a semiconductor device upon which the carrier substrate is to be fabricated, adjacent the bond pads thereof. Laterally extending conductive lines are fabricated on the layer of insulative material and in contact with corresponding bond pads of the semiconductor device. Conductive bumps are then disposed adjacent corresponding conductive lines and a layer of polymeric material applied to the semiconductor device so as to insulate the conductive lines. The conductive bumps are exposed through the layer of polymeric material. Since each of the conductive lines of the carrier substrate of the '304 Patent extends substantially laterally from its corresponding bond pad, each of the conductive bumps is, somewhat undesirably, laterally offset from the location of its corresponding bond pad. Moreover, the disposal of an additional layer of insulative material on the active surface of the semiconductor device, through which the bond pads are disposed, increases fabrication time and costs, as well as the likelihood of device failure.

**[0010]** As the carrier substrate of such chip-scale packages is small, electrical connections between the semiconductor device and the carrier substrate are often made by flip-chip-type bonds or tape-automated bonding ("TAB"). Due to the typical use of a carrier

substrate that has a different coefficient of thermal expansion than the semiconductor substrate of the semiconductor device, these types of bonds may fail during operation of the semiconductor device.

**[0011]** Following packaging, the packaged semiconductor devices may be re-tested or otherwise processed to ensure that no damage occurred during packaging. The testing of individual packaged semiconductor devices is, however, somewhat undesirable since each package must be individually aligned with such testing or probing equipment.

**[0012]** Accordingly, there is a need for a chip-scale package with at least some conductive bumps or contacts that are not laterally offset from the position of their corresponding bond pad and for a packaging method that does not require the disposal of an additional layer of insulative material adjacent the active surface of the semiconductor device. There is also a need for a semiconductor packaging process that facilitates testing, probing, and burn-in of semiconductor devices without requiring the alignment of individual semiconductor devices and by which a plurality of reliable chip-scale packages may be substantially simultaneously assembled. An efficient chip-scale packaging process with a reduced incidence of semiconductor device failure is also needed. There is a further need for chip-scale packaged semiconductor devices that consume about the same amount of real estate as the semiconductor devices thereof and that withstand repeated exposure to the operating conditions of the semiconductor device.

#### SUMMARY OF THE INVENTION

**[0013]** The present invention includes a chip-scale package (“CSP”) including a semiconductor device having at least one bond pad on an active surface thereof and a carrier substrate, which is also referred to herein as a carrier, adjacent the active surface of the semiconductor device and including at least one electrically conductive via therethrough. The at least one electrically conductive via preferably extends directly through or substantially longitudinally through the carrier substrate and is alignable with the at least one bond pad of the semiconductor device. The carrier substrate may also include at least one conductive bump in communication with the at least one electrically conductive via and disposed opposite the semiconductor device. The at least one electrically conductive bump may be disposed adjacent

the at least one electrically conductive via. Alternatively, the carrier substrate may carry at least one conductive trace that extends substantially laterally from the at least one electrically conductive via. The at least one conductive bump may be disposed in contact with the at least one electrically conductive trace and, therefore, the at least one electrically conductive bump may be laterally offset from its corresponding bond pad of the semiconductor device.

[0014] Preferably, the carrier substrate comprises a layer of polymeric material, such as a polyimide. The polymeric material is preferably disposed in a thickness or has a coefficient of thermal expansion that will not induce stress in the conductive links between the semiconductor device and the carrier substrate under the operating conditions of the semiconductor device (e.g., the operating temperature of the semiconductor device). Accordingly, in accordance with the method of the present invention, the carrier substrate may be secured to the active surface of the semiconductor device by disposing and spreading a quantity of polymeric material on the active surface of the semiconductor device to a substantially consistent thickness. Alternatively, a preformed film of the polymeric material may be adhered or otherwise secured to the active surface of the semiconductor device. The layer of polymeric material may be disposed on the semiconductor device either before or after the semiconductor device has been singulated from a wafer.

**[0015]** Apertures may be defined through the layer of polymeric material by known processes, such as by laser-drilling, by masking and etching, or by photoimaging the layer of polymeric material. These apertures may be defined after the layer of polymeric material has been secured to the active surface of the semiconductor device. Alternatively, if a preformed film of polymeric material is secured to the active surface of the semiconductor device, the apertures may also be preformed. If the layer of polymeric material comprises a preformed film of polymeric material having preformed apertures therethrough, each aperture is preferably substantially alignable with its corresponding bond pad of the semiconductor device as the polymeric film is secured to the active surface of the semiconductor device.

[0016] A quantity of conductive material may be disposed in each aperture of the layer of polymeric material and, therefore, in contact with the bond pad that corresponds to the

aperture. Each aperture and the quantity of conductive material therein collectively define a conductive via of the carrier substrate.

**[0017]** Conductive traces that extend substantially laterally from selected ones of the electrically conductive vias may also be fabricated on the carrier substrate, opposite the semiconductor device. Preferably, these conductive traces are positioned to laterally offset the locations of contacts or conductive bumps of the carrier substrate relative to the locations of their corresponding bond pads of the semiconductor device. Accordingly, the conductive traces may impart the carrier substrate with a footprint that differs from that of the semiconductor device to which the carrier substrate is secured.

**[0018]** Conductive bumps may be disposed on a surface of the carrier substrate opposite the semiconductor device. Each conductive bump preferably communicates with at least one corresponding bond pad of the semiconductor device. Accordingly, the conductive bumps may be disposed in contact with either an electrically conductive via or a substantially laterally extending conductive trace of the carrier substrate.

**[0019]** Other features and advantages of the present invention will become apparent to those of ordinary skill in the art through a consideration of the ensuing description, the accompanying drawings, and the appended claims.

#### BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

**[0020]** FIG. 1 is a cross-sectional representation of a first embodiment of a chip-scale package according to the present invention;

**[0021]** FIG. 1A is a cross-sectional representation of another embodiment of a chip-scale package according to the present invention;

**[0022]** FIG. 2 is a cross-sectional representation of a semiconductor device having a layer of polymeric material secured to an active surface thereof;

**[0023]** FIG. 2A is a cross-sectional representation of a semiconductor device having a layer of polymeric material secured to an active surface thereof and a quantity of polymeric material adjacent a peripheral edge thereof;



**[0024]** FIG. 2B is a schematic representation of a wafer including a plurality of semiconductor devices thereon and a layer of polymeric material disposed over the active surfaces of the semiconductor devices;

**[0025]** FIG. 3 is a cross-sectional representation of the semiconductor device of FIG. 2, illustrating apertures defined through the layer of polymeric material;

**[0026]** FIG. 4 is a cross-sectional representation of the semiconductor device of FIG. 3, illustrating conductive material disposed within the apertures to form electrically conductive vias;

**[0027]** FIG. 4A is a cross-sectional representation of the semiconductor device of FIG. 4, illustrating substantially laterally extending conductive traces in communication with the conductive material disposed in selected ones of the apertures, which conductive material forms electrically conductive vias;

**[0028]** FIG. 4B is a cross-sectional representation of the semiconductor device of FIG. 3, illustrating an alternative method of disposing conductive material within the apertures of the carrier substrate to form electrically conductive vias and conductive bumps;

**[0029]** FIG. 4C is a cross-sectional representation of the semiconductor device of FIG. 4B, illustrating the disposal of another layer of polymeric material laterally adjacent the conductive bumps;

**[0030]** FIG. 5 is a cross-sectional representation of the semiconductor device of FIG. 4, illustrating contact pads disposed in communication with the conductive material of the electrically conductive vias;

**[0031]** FIG. 5A is a cross-sectional representation of the semiconductor device of FIG. 4A, illustrating contact pads disposed in communication with the conductive material of the electrically conductive vias and the conductive traces;

**[0032]** FIG. 6 is a cross-sectional representation of the semiconductor device of FIG. 5, illustrating conductive bumps disposed in communication with the conductive material within the apertures;

**[0033]** FIG. 6A is a cross-sectional representation of the semiconductor device of FIG. 5A, depicting conductive bumps in communication with selected ones of the substantially laterally extending conductive traces;

**[0034]** FIG. 6B is a cross-sectional representation of the semiconductor device of FIG. 4C, illustrating the disposal of a layer of conductive elastomer over the conductive bumps;

[0035] FIG. 6C is a cross-sectional representation of the semiconductor device of FIG. 4C, illustrating the disposal of a layer of conductive elastomer including laterally extending conductive regions over the conductive bumps;

[0036] FIG. 6D is a cross-sectional representation of the semiconductor device of FIG. 6A, illustrating the disposal of another layer of polymeric material laterally adjacent the conductive bumps;

[0037] FIG. 7 is a schematic representation of the singulation of chip-scale packages from a wafer including a plurality of chip-scale packages;

[0038] FIG. 8A is a cross-sectional representation of another embodiment of a chip-scale package according to the present invention, which includes a semiconductor device having bond pads in a leads over chip (“LOC”) type arrangement;

[0039] FIG. 8B is a schematic representation of the top of the chip-scale package of FIG. 8A;

[0040] FIG. 8C is a schematic representation of the top of a variation of the chip-scale package of FIG. 8A, which includes groups of external package bumps that correspond to single bond pads of the semiconductor device;

[0041] FIG. 8D is a cross-sectional representation of another variation of the chip-scale package of FIG. 8A, which includes a semiconductor device having peripherally disposed bond pads:

[0042] FIG. 9A is a cross-sectional representation of another embodiment of the chip-scale package of the present invention, which includes a semiconductor device having peripherally disposed bond pads;

[0043] FIG. 9B is a cross-sectional representation of a variation of the chip-scale package of FIG. 9A, wherein the bond pads of the semiconductor device are disposed in a LOC-type arrangement; and

**[0044]** FIGs. 10A and 10B are cross-sectional representations of another embodiment of the chip-scale package, wherein the carrier substrate includes regions of conductive elastomer therethrough.

## DETAILED DESCRIPTION OF THE INVENTION

[0045] With reference to FIG. 1, a preferred embodiment of a chip-scale package 10 (“CSP”) according to the present invention is illustrated. Chip-scale package 10 includes a semiconductor device 12 and a carrier substrate 18 disposed adjacent an active surface 14 of semiconductor device 12.

**[0046]** Semiconductor device 12 is preferably a flip-chip-type semiconductor device, including bond pads 16 disposed on active surface 14 thereof in either an array thereover or proximate the periphery of semiconductor device 12. However, semiconductor devices that include peripherally located bond pads are also within the scope of the present invention.

[0047] Carrier substrate 18 comprises a polymeric material, such as a polyimide, and has a substantially consistent thickness. Carrier substrate 18 includes electrically conductive vias 21, which are also referred to herein as vias for simplicity, extending therethrough and in communication and substantial alignment with their corresponding bond pads 16. As illustrated, carrier substrate 18 may also include conductive traces 22 that extend substantially laterally from selected ones of electrically conductive vias 21 and that communicate with their corresponding electrically conductive vias 21. These conductive traces 22 extend substantially laterally from their corresponding electrically conductive vias 21 and may be carried on a surface of carrier substrate 18 opposite semiconductor device 12 or may otherwise be carried by carrier substrate 18. Carrier substrate 18 may also have electrically conductive bumps 24 disposed in communication with corresponding electrically conductive vias 21. These electrically conductive bumps 24 may be disposed adjacent their corresponding electrically conductive vias 21 or in contact with conductive traces 22 that correspond to their corresponding electrically conductive vias 21. The conductive bumps 24 may be disposed in direct contact with their corresponding electrically conductive via 21 or conductive trace 22. Alternatively, conductive bumps 24 may be disposed in communication with their corresponding electrically conductive via 21 or conductive

trace 22 by means of a pad 23 of ball-limiting metallurgy (“BLM”) or under-bump metallurgy (“UBM”) of a type known in the art (see FIGs. 5-6A).

**[0048]** FIG. 1A illustrates another embodiment of a chip-scale package 110 according to the present invention. Chip-scale package 110 includes a semiconductor device 112 with bond pads 116 disposed on an active surface 114 thereof. A carrier substrate 118 disposed adjacent active surface 114 of semiconductor device 112 may include one or more layers 118a, 118b of polymeric material. Apertures 120 that are defined through carrier substrate 118 are preferably substantially alignable with corresponding bond pads 116 of semiconductor device 112. Each aperture 120 preferably includes a quantity of conductive material therein. Each aperture 120 and the conductive material therein collectively define an electrically conductive via 121, which may extend substantially through carrier substrate 118. A layer 126 of elastomer is disposed adjacent backside 119 of carrier substrate 118. Layer 126 includes conductive regions 127, such as regions of a conductive elastomer (e.g., a z-axis elastomer) surrounded by non-conductive elastomer 125, that correspond substantially to and are substantially alignable with corresponding electrically conductive vias 121 or other corresponding electrically conductive features of carrier substrate 118. Conductive regions 127 may extend laterally beyond the peripheries of their corresponding electrically conductive vias 121 or other electrically conductive features of carrier substrate 118. Accordingly, conductive regions 127 may facilitate the electrical connection of semiconductor device 112 to a substrate that includes contact pads disposed in a different footprint than that of bond pads 116 of semiconductor device 112. Chip-scale package 110 may also include conductive bumps 124 adjacent conductive regions 127 of layer 126. A protective layer 128 may be disposed adjacent layer 126 and laterally adjacent to any conductive bumps 124. Protective layer 128 may protect layer 126 and provide support for conductive bumps 124.

**[0049]** With reference to FIG. 2, carrier substrate 18 may be disposed on active surface 14 of semiconductor device 12 by known processes. For example, a quantity of polymeric material, such as a polyimide, an epoxy, parylene, a fluoropolymer, or a photoresist, may be disposed on active surface 14 and spread to a substantially uniform thickness, in order to define carrier substrate 18. The quantity of polymeric material may be spread by known processes, such as by spin-on techniques or by mechanical means, such as the use of a doctor blade.

**[0050]** Alternatively, a preformed sheet of polymeric material may be secured to active surface 14 of semiconductor device 12. Preferably, if such a preformed sheet of polymeric material is employed as carrier substrate 18, the preformed sheet is secured to active surface 14 by means of an adhesive material. Alternatively, the preformed sheet of polymeric material may be heated to secure the same to active surface 14 of semiconductor device 12.

**[0051]** As another alternative, the polymer of carrier substrate 18 may comprise a durable polymeric material which can be applied to a semiconductor device in a layer having a thickness of up to about one mil (25 microns) or greater and which may be formed into desired shapes of very fine resolution (i.e., about  $1\mu\text{m}$  and lower) by photoimaging processes. Some photoimageable epoxies are useful as the polymer of carrier substrate 18. One such material is the multi-functional glycidyl ether derivative of bisphenol-A novolac high-resolution negative photoresist available from Shell Chemical Company of Houston, Texas under the trade name EPON® SU-8. EPON® SU-8 is a low molecular weight resin which is useful for fabricating structures having dimensions in the lower range of about  $0.25\mu\text{m}$  to about  $0.10\mu\text{m}$ . As employed in the present invention, however, the multi-functional glycidyl ether derivative of bisphenol-A novolac is useful for forming layers of up to about  $250\mu\text{m}$  (10 mils) thick. When combined with a photoinitiator, or promoter, the photoimageable epoxy forms a highly structured, cross-linked matrix. One such photoinitiator is triaryl sulfonium salt, which is available from Union Carbide Corporation of Danbury, Connecticut under the trade name CYRACURE® UVI. That highly structured, cross-linked matrix may then be solvated in organic solvents such as gamma-butyrolactone, propylene glycol methyl ether acetate, and methyl iso-butyl ketone. Other photoinitiators are also useful for forming such cross-linked matrices with multi-functional glycidyl ether derivatives of bisphenol-A novolac such as EPON® SU-8.

**[0052]** Upon solvation of the photoimageable epoxy, a desired thickness of the photoresist-photoinitiator compound is applied to active surface 14 of semiconductor device 12 by known methods, such as by spin-coating or spraying. The compound layer may be masked by known processes and cross-linked by exposure to radiation to define apertures 20 therethrough. Radiation sources which are useful for cross-linking overcoat layers which include a multi-functional glycidyl ether derivative of bisphenol-A novolac include, without limitation, ultraviolet

radiation, electron-beam radiation, and X-ray radiation. Due to the transparency of the multi-functional glycidyl ether derivative of bisphenol-A novolac that is useful in the present invention, photoimaging of carrier substrate 18 defines apertures 20 having substantially perpendicular walls. The excess material is then removed from the semiconductor device by known methods. Other materials, including other ultraviolet, X-ray, electron-beam, and laser-imageable materials may be employed to fabricate carrier substrate 18. For example, photoimageable polyimides and other photoimageable materials which are not fully transparent may be used to fabricate carrier substrate 18.

**[0053]** The polymeric material employed as carrier substrate 18 will preferably withstand the temperatures and other conditions that may be subsequently employed to fabricate or assemble chip-scale package 10. For example, the polymeric material of carrier substrate 18 should withstand any metallization processes that are subsequently employed to fabricate electrically conductive vias 21 (see FIGs. 1 & 1A), conductive traces 22 (see FIGs. 1 & 1A), and any ball-limiting metallurgy such as that of pads 23 (see FIGs. 5-6A), as well as the increased temperatures typically associated with disposing conductive bumps, such as solder bumps, proximate thereto. The polymeric material of carrier substrate 18 will also preferably maintain its integrity and otherwise withstand conditions to which carrier substrate 18 is exposed during any masking or patterning of structures on either carrier substrate 18 or semiconductor device 12. For example, the polymeric material of carrier substrate 18 should withstand exposure to photomasked chemicals, as well as any etchants to which carrier substrate 18 may be exposed.

**[0054]** The polymeric material of carrier substrate 18 preferably has a similar coefficient of thermal expansion to that of the materials of active surface 14 of semiconductor device 12 so as to minimize the likelihood of stress related failure of the electrical links between semiconductor device 12 and carrier substrate 18. Alternatively, the polymeric material of carrier substrate 18 may have a thickness that minimizes the likelihood of such stress related failure.

**[0055]** Referring to FIG. 2A, the polymeric material of carrier substrate 18 may also be disposed adjacent a peripheral edge 15 of semiconductor device 12. As an example, if a preformed film of polymeric material is employed as carrier substrate 18, portions of the film of polymeric material may be wrapped so as to be disposed against and secured to peripheral

edge 15. If the polymeric material of carrier substrate 18 is spread to a substantially uniform thickness following its disposal on active surface 14 of semiconductor device 12 and semiconductor device 12 has already been singulated from a wafer, some of the polymeric material may be permitted to flow around peripheral edge 15 and may, thereby, be disposed adjacent peripheral edge 15.

**[0056]** With reference to FIG. 2B, carrier substrate 18 may be secured to semiconductor device 12 on a wafer scale. Stated another way, a layer of polymeric material, which comprises carrier substrate 18, may be disposed on a wafer 30 that includes a plurality of semiconductor devices 12 (see FIGs. 1, 2, and 2A), which wafer is also referred to herein as a semiconductor device wafer.

**[0057]** Referring now to FIG. 3, apertures 20 may be formed through carrier substrate 18. Preferably, apertures 20 extend substantially longitudinally through carrier substrate 18 and are substantially alignable with corresponding bond pads 16 of semiconductor device 12. Apertures 20 may either be preformed through carrier substrate 18 by known processes (e.g., mechanically or laser-drilled), formed after carrier substrate 18 has been secured to active surface 14 of semiconductor device 12, or defined during the fabrication of carrier substrate 18, such as by the photoimaging processes disclosed above in reference to the use of photoimageable epoxies as carrier substrate 18.

**[0058]** If apertures 20 are formed through carrier substrate 18 after carrier substrate 18 has been secured to active surface 14, known processes may be employed to define apertures 20. For example, mask and etch techniques may be employed to define apertures 20 through carrier substrate 18. Alternatively, known laser-drilling processes may be employed to define apertures 20. As another alternative, apertures 20 may be defined by known mechanical drilling processes.

**[0059]** Referring to FIG. 4, conductive material may be disposed in each of apertures 20 in order to define electrically conductive vias 21 through carrier substrate 18. Preferably, electrically conductive vias 21 are each positioned to align substantially with a corresponding bond pad 16 of semiconductor device 12. Known processes may be employed to fabricate electrically conductive vias 21. For example, a quantity of conductive material, such as a metal,

may be disposed over carrier substrate 18, including within the apertures 20 thereof. The conductive material may be disposed on a backside 19 of carrier substrate 18 by known processes, such as by physical vapor deposition (“PVD”) (e.g., sputtering) or chemical vapor deposition (“CVD”) processes. As these processes typically blanket deposit a layer of conductive material onto a surface, it may be necessary to pattern the layer of conductive material. Known techniques, such as the use of a photo mask and etching processes, may be employed to remove conductive material substantially from backside 19 of carrier substrate 18.

**[0060]** Turning now to FIG. 4A, conductive traces 22, which extend substantially laterally from selected ones of electrically conductive vias 21, may be fabricated so as to be carried by carrier substrate 18. Preferably, these conductive traces 22 are disposed on backside 19 of carrier substrate 18. Alternatively, conductive traces 22 may extend, at least partially, internally through carrier substrate 18. Each conductive trace 22 preferably communicates with a corresponding electrically conductive via 21 of carrier substrate 18 and, therefore, with a corresponding bond pad 16 of semiconductor device 12. Since conductive traces 22 extend substantially laterally from their corresponding electrically conductive vias 21, conductive traces 22 of carrier substrate 18 are useful for establishing electrical connections between the contacts of a substrate and bond pads 16 of a semiconductor device 12 having a different footprint than that of the substrate.

**[0061]** If electrically conductive vias 21 were fabricated by a technique that employed a blanket-deposited layer of conductive material, conductive traces 22 may be defined from the layer of conductive material as the layer of conductive material is patterned to define electrically conductive vias 21. Alternatively, conductive traces 22 may be fabricated at a different time than electrically conductive vias 21 are fabricated. Again, conductive traces 22 may be fabricated by known processes, such as by disposing a layer of conductive material on backside 19 of carrier substrate 18 and removing selected regions of the layer of conductive material to pattern the same and to define conductive traces 22 therefrom. Known mask and etch processes may be employed to pattern the conductive layer.

**[0062]** Alternatively, with reference to FIG. 4B, which illustrates the fabrication of package 110, electrically conductive vias 121 may be fabricated by disposing the solder within

apertures 120. Solder may be disposed within apertures 120 by known processes, such as by wave solder processes, by disposing a molten solder ball adjacent or in each aperture 120, or by disposing a solder brick within or adjacent to each aperture 120 and heating the solder brick to reflow the same. Preferably, as molten solder is disposed within each aperture 120, an electrically conductive via 121 is formed and substantially concurrently bonded to a corresponding bond pad 116 of semiconductor device 112.

**[0063]** When solder is employed as the conductive material of electrically conductive vias 121, if the solder protrudes beyond backside 119 of carrier substrate 118, it may be necessary to dispose an additional quantity of polymeric material on backside 119. As illustrated FIG. 4C, a second substrate layer 118b may be disposed on backside 119 of carrier substrate 118. Second substrate layer 118b may be disposed by known processes, such as by the processes explained above in reference to FIGs. 2 and 2A. Subsequent processes may then be performed on a backside 119b of second substrate layer 118b, including those processes that are explained in reference to backside 119 of carrier substrate 118.

**[0064]** With reference to FIGs. 5 and 5A, a pad 23, 23' may be fabricated in contact or otherwise in communication with a corresponding electrically conductive via 21 or conductive trace 22. If such a pad 23 is employed, the use of known ball-limiting metallurgy (“BLM”) or under-bump metallurgy (“UBM”) structures is preferred. Pad 23, 23' may be fabricated by known processes, such as the processes that are typically employed to fabricate ball-limiting metallurgy structures (e.g., fabricating layers by PVD and patterning the layers by mask and etch processes). Accordingly, each pad 23, 23' may include an adhesion layer adjacent the conductive material of its corresponding electrically conductive via 21 or conductive element 22, a solder wetting layer adjacent the adhesion layer, and an exposed, substantially non-oxidizable protective layer (e.g., gold or other noble metal) adjacent the solder wetting layer.

**[0065]** FIGs. 8A and 8B illustrate another embodiment of a chip-scale package 210, which includes a semiconductor device 212 and a carrier substrate 218 disposed adjacent an active surface 214 of semiconductor device 212.

**[0066]** As illustrated, semiconductor device 212 is a leads over chip (“LOC”) type semiconductor device, which includes bond pads 216 disposed substantially linearly across the

center of semiconductor device 212. A conductive bump 217 may be disposed on each bond pad 216 or on a BLM or UBM structure adjacent to each bond pad 216.

[0067] Carrier substrate 218 comprises an insulative layer 220, preferably formed of polymeric material, such as polyimide or another non-conductive elastomer, and has a substantially consistent thickness. Bond pads 216 of semiconductor device 212 or conductive bumps 217 are exposed through layer 220 through one or more apertures 228. An adhesive film layer 230 is disposed adjacent layer 220, opposite semiconductor device 212. Adhesive film layer 230 carries conductive traces 222 and external package bumps 224. External package bumps 224 protrude from adhesive film layer 230. Conductive traces 222 are in electrical communication with corresponding external package bumps 224 and extend across adhesive film layer 230 to corresponding vias 221. Vias 221, which communicate with conductive traces 222, extend through adhesive film layer 230, into apertures 228, and into electrical communication with corresponding bond pads 216.

**[0068]** As illustrated in FIGS. 8A and 8B, each conductive trace 222 communicates with a corresponding external package bump 224. Thus, each bond pad 216 that communicates with a conductive trace 222 may also communicate with a laterally offset, corresponding external package bump 224. Alternatively, as illustrated in FIG. 8C, each conductive trace 222 may communicate with a group or an array of external package bumps 224'.

[0069] FIG. 8D illustrates a variation of chip-scale package 210', which includes a semiconductor device 212' having peripherally located bond pads 216' and external package bumps 224' disposed in an array on adhesive film layer 230'.

**[0070]** With reference to FIG. 9A, another embodiment of a chip-scale package 310 according to the present invention is illustrated. Chip-scale package 310 includes a semiconductor device 312 having bond pads 316 disposed on an active surface 314 of semiconductor device 312, adjacent the periphery thereof. Selected bond pads 316 have conductive bumps 317 adjacent thereto.

**[0071]** A carrier substrate 318 is disposed adjacent active surface 314. Carrier substrate 318 includes an insulative layer 320, preferably formed of an electrically non-conductive polymeric material, such as polyimide or another elastomer, and has a substantially uniform

thickness. Insulative layer 320 includes apertures 328 formed therethrough to receive conductive bumps 317. Preferably, conductive bumps 317 have a height substantially equal to or greater than the thickness of insulative layer 320.

**[0072]** An adhesive film layer 330 is disposed adjacent insulative layer 320, opposite semiconductor device 312. Adhesive film layer 330 carries electrically conductive traces 322 and external package bumps 324, which protrude from adhesive film layer 330. Electrically conductive traces 322 are disposed across adhesive film layer 330 so as to extend between, to electrically contact, and to facilitate electrical communication between a conductive bump 317 and one or more corresponding external package bumps 324.

**[0073]** FIG. 9B illustrates a variation of chip-scale package 310', wherein the semiconductor device 312' is a LOC-type device having bond pads 316' disposed substantially linearly across the center of the active surface 314' thereof.

**[0074]** FIGs. 9A and 9B illustrate chip-scale packages 310, 310' that rearrange the peripheral and LOC-type footprints of semiconductor devices 312, 312' to provide array-type footprints of external package bumps 324, 324'.

**[0075]** The chip-scale packages 210, 210', 310, 310' illustrated in FIGs. 8A-9B and the features thereof may be fabricated by processes that are known in the art, such as by the processes described above with reference to FIGs. 1-5A.

**[0076]** Referring now to FIGs. 6 and 6A, conductive bumps 24 may be disposed in contact or otherwise in communication with electrically conductive vias 21 or conductive traces 22. If carrier substrate 18 includes any pads 23, 23', conductive bumps 24 are preferably disposed adjacent such pads 23, 23'. Conductive bumps 24 may comprise any electrically conductive material known in the art to be useful as a conductive joint between adjacent devices. Exemplary materials include, without limitation, solders, electrically conductive elastomers (e.g. z-axis elastomers), z-axis tapes, and other electrically conductive materials and structures. Known processes may be employed to fabricate conductive bumps 24 from these materials and in communication with selected ones of electrically conductive vias 21 of carrier substrate 18.

[0077] Alternatively, with reference to FIGS. 6B and 6C, which illustrate the fabrication of package 110, if carrier substrate 118 does not include conductive traces extending across backside 119 thereof or if only a contact region (see, e.g., reference 22a of FIG. 1) of each conductive trace (see, e.g., reference 22 of FIG. 1) of carrier substrate 118 is exposed to backside 119, a substantially planar layer 126 comprising a non-conductive elastomer 125 having therein localized conductive regions 127 of a conductive elastomer, such as a z-axis elastomer or anisotropic conductive elastomer of a type known in the art, may be disposed adjacent backside 119 of carrier substrate 118. The conductive regions 127 of such a substantially planar layer 126 preferably contact each electrically conductive via 121 or contact region (see, e.g., reference 22a of FIG. 1) of a conductive element (not shown in FIG. 6A or 6B) to facilitate the transmission of electrical signals through each electrically conductive via 121 of carrier substrate 118 to or from bond pads 116. Substantially planar layer 126 may be disposed on backside 119 of carrier substrate 118 by known processes, such as by securing a preformed layer of elastomer having conductive regions 127 therein to backside 119. Alternatively, a quantity of non-conductive elastomer 125 may be disposed on backside 119 and spread to a substantially uniform thickness thereacross by known techniques, such as by spin-on processes or mechanical processes (e.g., the use of a doctor blade), electrically conductive vias 121 exposed through non-conductive elastomer 125, and an electrically conductive elastomer disposed adjacent electrically conductive vias 121 so as to form conductive regions 127 peripherally surrounded by non-conductive elastomer 125. The conductive components of a conductive elastomer disposed in this manner may also be aligned by known processes, such as by magnetically aligning the conductive components.

**[0078]** Of course, with reference to FIG. 6C, conductive regions 127 of substantially planar layer 126 may extend laterally beyond the peripheries of their corresponding electrically conductive vias 121 or beyond the contact regions of their corresponding conductive traces (see, e.g., reference 22 of FIG. 1).

**[0079]** With reference to FIG. 6D, a protective layer 28 of polymeric material may be disposed adjacent backside 19 of carrier substrate 18 and laterally adjacent conductive bumps 24 protruding therefrom. Protective layer 28 may also be disposed laterally adjacent or cover

conductive traces 22. Protective layer 28 preferably provides lateral support for conductive bumps 24. Known processes may be employed to dispose protective layer 28 on backside 19 of carrier substrate 18, such as disposing a quantity of polymeric material on backside 19 and permitting the polymeric material to flow around conductive bumps 24 such that conductive bumps 24 remain exposed through protective layer 28. Alternatively, protective layer 28 may be disposed in a substantially uniform thickness on backside 19 of carrier substrate 18 by spin-on processes. Materials that may be employed as protective layer 28 include, without limitation, polyimides and photoresist materials.

**[0080]** As the chip-scale packages 10 of the present invention may be fabricated on a wafer scale, as depicted in FIG. 2B, testing, probing, or burn-in of each of the semiconductor devices 12 of wafer 30 can be performed after packaging, but while the semiconductor devices are still in wafer form. Thus, the packaging method of the present invention eliminates the need to individually align individually packaged semiconductor devices with test equipment.

**[0081]** FIGs. 10A and 10B illustrate an embodiment of chip-scale package 410 wherein a carrier substrate 418 includes an insulative layer 430 of a material such as polyimide or another elastomer disposed adjacent an active surface 414 of a semiconductor device 412.

**[0082]** Apertures 428 are formed through insulative layer 430 by known processes, such as by the etching, laser-drilling, or other processes disclosed above with reference to FIGs. 1-6D, to exposed bond pads 416 of semiconductor device 412. Of course, the processes that are employed to form apertures 428 and the sequence in which these processes are performed (i.e., before or after insulative layer 430 is disposed on semiconductor device 412) depend upon the type of material or materials from which insulative layer 430 is fabricated.

**[0083]** A quantity of conductive elastomer 421, such as a z-axis conductive elastomer, is disposed within each aperture 428 to facilitate the electrical communication of each bond pad 416 with a structure positioned on an opposite side of or carried by carrier substrate 418. For example, as illustrated in FIG. 10B, a BLM or UBM pad 440 may be disposed adjacent conductive elastomer 421. An external package bump 424 may then be disposed in contact with pad 440. Alternatively, conductive traces that communicate with external package bumps may be

disposed in electrical communication with conductive elastomer 421 so as to offset or rearrange the footprint of semiconductor device 412.

**[0084]** Turning now to FIG. 7, individual chip-scale packages 10 may be singulated from wafer 30 by known singulation processes, such as by the use of a wafer saw 40.

**[0085]** Although the foregoing description contains many specifics and examples, these should not be construed as limiting the scope of the present invention, but merely as providing illustrations of some of the presently preferred embodiments. Similarly, other embodiments of the invention may be devised which do not depart from the spirit or scope of the present invention. The scope of this invention is, therefore, indicated and limited only by the appended claims and their legal equivalents, rather than by the foregoing description. All additions, deletions and modifications to the invention as disclosed herein and which fall within the meaning of the claims are to be embraced within their scope.